August 16, 2002 TEES
ERRATUM 2
June 8, 2004

2.2.2.4
An EPROM Memory, INTEL 27256A or equal, shall be provide in socket U6.

5.1.3
Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs. The output shall have a minimum impedance of 2 Mega Ohms when no vehicle is detected. The output shall be compatible with both Model 170 and 2070 controller unit inputs.

5.3.1.1
Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 57 mm maximum in diameter, have no sharp edges, and its length not to exceed 450 mm (18 in). The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a 30.8 m (100 ft) lead-in cable. Leakage resistance shall be a minimum of 10 megohms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 20 degrees (+/- 3 degrees) C. The salt water bath concentrate shall be one fourth ounce of salt per gallon of water.

9.1.5
2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-1B CPU	1.0 A	250mA		
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A&B FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	500 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6 All Comm	500 mA	-----	100 mA	100 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA

9.2.2.4
The 2070-1B CPU shall not draw more than 1.00 A of +5VDC & 250 mA of ISO+12 VDC.

9.2.3.5 FLASH MEMORY

A minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory shall be used for the Boot Image and a minimum of 6 MB shall be available for AGENCY use. The 2 MB of FLASH Memory shall be reserved the Boot Image only. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better."

9.2.6 DATA KEY

A Datakey Keyceptacle™ (KC4210, KC4210PCB or equal) shall be mounted on the CPU module front panel (or the Transition Board of MODEL 1A). Power shall not be applied to the receptacle if the key is not present.

The contractor shall supply a 2Mb Memory Size Datakey (SFK2Mb or equal) with each MODEL 1A TB (Transition Board) or 1B CPU module unless specified otherwise. The Datakey shall be temperature rated for –40 to +80 °C operation, shall be black in color, and shall be initialized to the format and default values defined below.

When programmed, the memory on the key of header version 1 shall be organized as follows:

Bytes	Description	Default Values
1-2	16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64	
3	Key Type	See table below
4	Header Version	2
5-8	Latitude	0.0
9-12	Longitude	0.0
13-14	Controller ID	0xFFFF
15-16	Communication drop number	0xFFFF
17-20	IP Address	10.20.70.51
21-24	Subnet Mask	255.255.255.0
25-28	Default Gateway	10.20.70.254
29	Startup Override	0xFF
20-64	Reserved for Agency use	All bytes set to 0xFF
65 to End	User Data	All bytes set to 0xFF

When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:

Key Type	Model No.	Memory Size	Sector Size
1	DK1000	1Kb	1 Byte
2	LCK16000	16Kb	1 Byte
3	SFK2Mb	2Mb	64KBytes
4	TBD	4Mb	64KBytes
5	TBD	8Mb	64KBytes

The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD. All the other fields shall follow a Big Endian Format as implemented by Motorola CPUs.

The Startup Override byte may be used to override the default controller startup procedure, as described in section 9.2.7.3.3.

9.2.7.1 OPERATING SYSTEM

The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.2 or later with kernel edition #372 or later. The following modules shall be included:

1. **Embedded OS-9 Real Time Kernel**
2. **Sequential Character File Manager (SCF)**
3. **Stacked Protocol File Manager (SPF)**
4. **Pipe File Manager (PIPEMAN)**
5. **Random Block File Manager (RBF)**
6. **C Shared Library (CSL)**

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Format	Dcheck	Login	Link	Kermit
Tsmon	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime	Merge	grep	

The Boot Image with the above utilities and including the network driver and descriptor shall be loaded into RAM as part of OS-9 initialization as defined in section 9.2.7.3.2.

9.2.7.2.3
A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Timer resolution shall be one count equals 100 µS and all timer periods shall be specified in units of hundreds of microseconds (µS), i.e. a timer period of 7 = 700µS. The minimum allowed timer period shall be 500µS. The maximum timer period for timers 1-4 shall be 6.5535 seconds (0xFFFf). The maximum timer period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E$Param from os_setstat() if the requested timer period is outside the allowable range.

A signal of "0" shall be an invalid signal and the driver shall return an E$PARAM error if received.

Access to the MC68360 internal timers shall be through the following descriptors:

9.2.7.2.3.3
Timer Extension to Standard OS-9 Function Calls:

The timer drivers shall support the following modes using the following function with the SS_2070 option code and a custom parameter block structure:

```
error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);
```

a) Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal.

```
pb→code = SS2070_Timer_Sig ;     /* request for one-shot signal */

pb→param1 = signal;
pb→param2.param = period;
```

b) Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

```
pb→code = SS2070_Timer_Cyc ;    /* request for periodic signal */

pb→param1 = signal;

pb→param2.param = period;
```

c) Start timer. Starts the timer if stopped, timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period. Timer will not send a signal and any pending signals will be cancelled.

pb→code = SS2070_Timer_Start; /* start timer if stopped */”

d) Stop timer. Leaves current value in timer and cancels any pending signals.

pb→code = SS2070_Timer_Stop; /* stop timer if running */

e) Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

pb→code = SS2070_Timer_Reset; /* reset timer (stop and zero) */

9.2.7.2.3.4
Timer Extension to Standard OS-9 Function Calls:

The timer driver shall support the following function with the SS_2070 option code and custom parameter block structure:

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);

a) Retrieve current timer configuration.

```
typedef struct
{
        u_int32 value;
        u_int32 mode;
        u_int32 signal;
        u_int32 period;
} Timer_status;

pb→code = GS2070_Status                 /* Request timer status data */
pb→param1 = sizeof(Timer_status)
pb→param2.pointer = &Timer_status
```

Status data shall be returned in the structure pointed to by pb→param2.pointer as follows:

pb→param2.pointer→value

pb→param2.pointer→mode /* SS2070_Timer_Sig if one-shot signal pending,
SS2070_Timer_Cyc if periodic signal pending,
SS2070_Timer_Start if free running,
SS2070_Timer_Stop if not active */

pb→param2.pointer→signal /* signal code pending if
SS2070_Timer_Sig or
SS2070_Timer_Cyc, 0 otherwise */

pb→param2.pointer→period /* timer period in µS x 100 if SS2070_Timer_Sig or SS2070_Timer_Cyc, 0 otherwise */

9.2.7.2.8

The FLASH drive shall be protected from corruption. It shall be protected using the Write Protect (WP) bit of the Base Register. This bit shall be set except when explicitly writing to flash. When writing to the FLASH drive the current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.

A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds.

9.2.7.2.10.2

The /f0/SYS shall contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user name "super" with password as "user" shall be defined in the password file.

A Termcap text file shall be include in the /f0/SYS directory. This Termcap file shall contain description fields defining the capability names and values of the front panel DISPLAY.

9.2.7.2.10.3

The utilities tar, make, vi, fixmod and mshell shall be included in the /f0/CMDS directory.

9.2.7.3.2

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 4 seconds. This startup time shall be measured from the release of SYSRESET to the turn on of the CPU LED using a user level program named ONLED. The ONLED program shall be the last module loaded into RAM and executed using opexec or a startup file.

9.2.7.3.3

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. **Sysgo shall set the execution directory to /f0wp/CMDS**

2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50s). If received, Sysgo shall:
   a. Fork a shell with no arguments on /sp4 using the current directory.
   b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.
3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid, Sysgo shall check the Startup Override byte in the Datakey header.
   If Startup Override is 0x01, Sysgo shall:
   a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be a 2-byte value indicating the length of the script. The script shall immediately follow the length value, and shall be stored as ASCII text.
   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.
   If Startup Override is 0x02, Sysgo shall:
   a. Fork an executable module stored on the Datakey immediately following the header.
   b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.
4. If the backspace key was not received and Startup Override was not performed:
   a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.
   b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.
5. If the backspace key was not received, Startup Override was not performed, and there is no OPEXEC file:
   a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.
   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

6. If the backspace key was not received, Startup Override was not performed, and there is no OPEXEC and no startup file:
   a. Sysgo shall fork a shell as described in step 2.

9.3.4 PARALLEL I/O PORTS

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground. The pull-up resistance shall not be less than 10K or more than 50 K Ohms.

9.3.5.2

An External WDT "Muzzle" Jumper shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 - Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to SET OUTPUTS Command. When the jumper is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.4.1

The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU LED, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A - FPA controller, two keyboards, AUX switch, alarm bell & Display A
OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell & Display B
OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60P.

9.4.3

The cathode of the CPU LED shall be electrically connected to the CPU LED signal and shall be pulled up to +5 VDC.

9.4.5.10

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

Tab stops shall be set based only upon the column (horizontal) position of the cursor; the row position shall be ignored. Each tab that is set shall applied to all rows of the display. In this way, tabs shall operate similarly to a typewriter or line printer. For example, if the cursor is positioned at column 21, row 3 when a Set Tab Stop command (ESC H) is received, a tab stop is placed at column 21 and applies to every row of the display. If the cursor is then positioned to column 21, row 5, and a Clear Tab Stop command (ESC[0g) is received, the tab stop on column 21 is removed and there will be no tab stop on any row of the display at that column position.

9.4.6
The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB, for 350±100 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

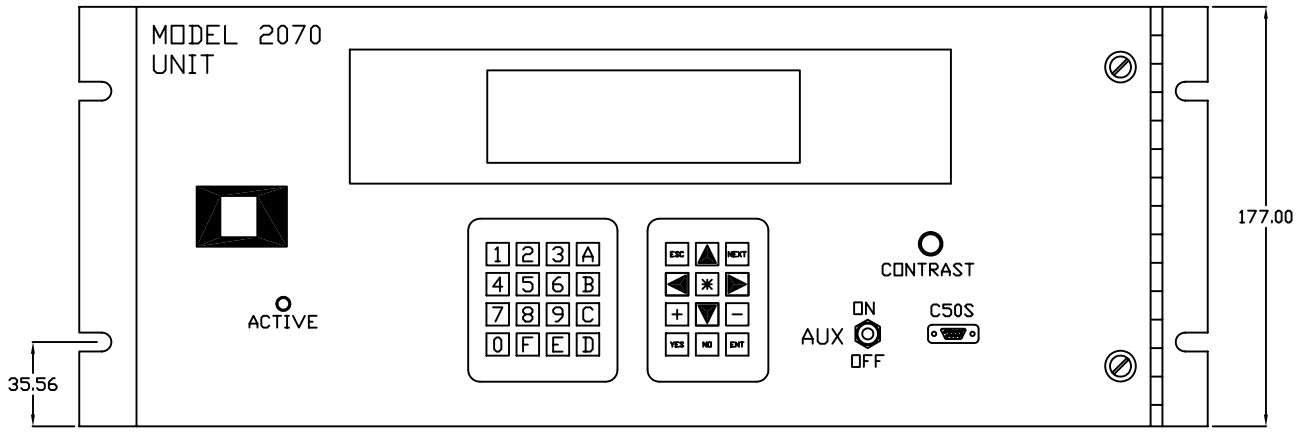
SPECIFICATION FOR MODEL 2070 PERIPHERAL EQUIPMENT

TABLE OF CONTENTS

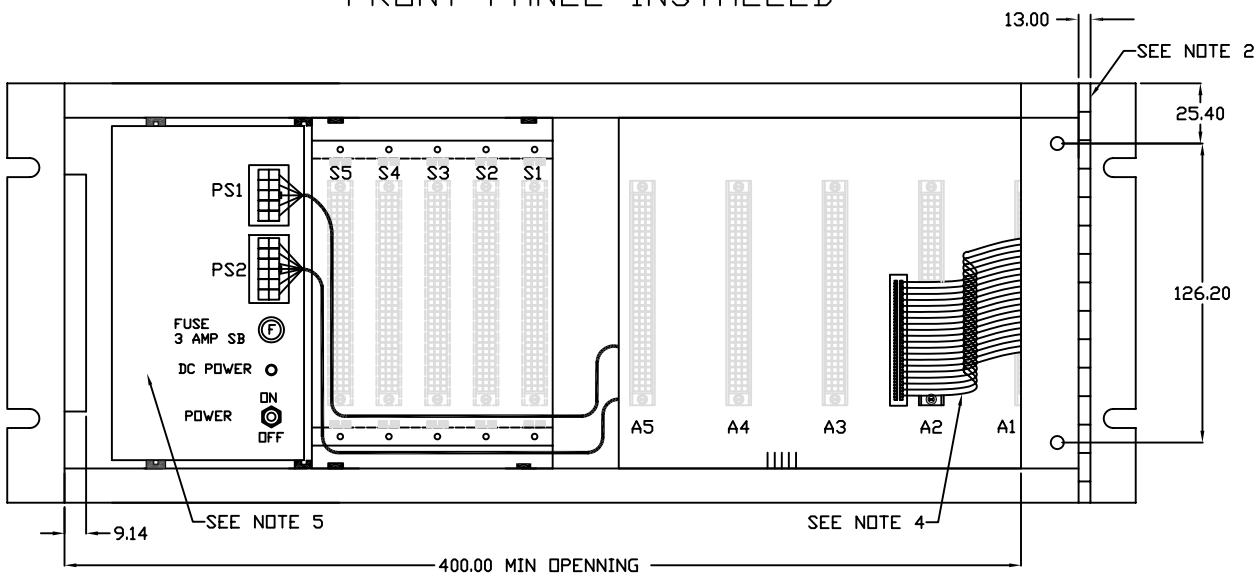
GENERAL NOTES:

1. **The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on the module.**
2. **Line drivers/receivers shall be socket or surface mounted.**
3. **Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.**
4. **The Comm modules shall be "Hot" swappable without damage to circuitry or operations.**

10.1.1
A fused isolated +5 VDC with a 100 mA power supply shall be provided for external use.
Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (4mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

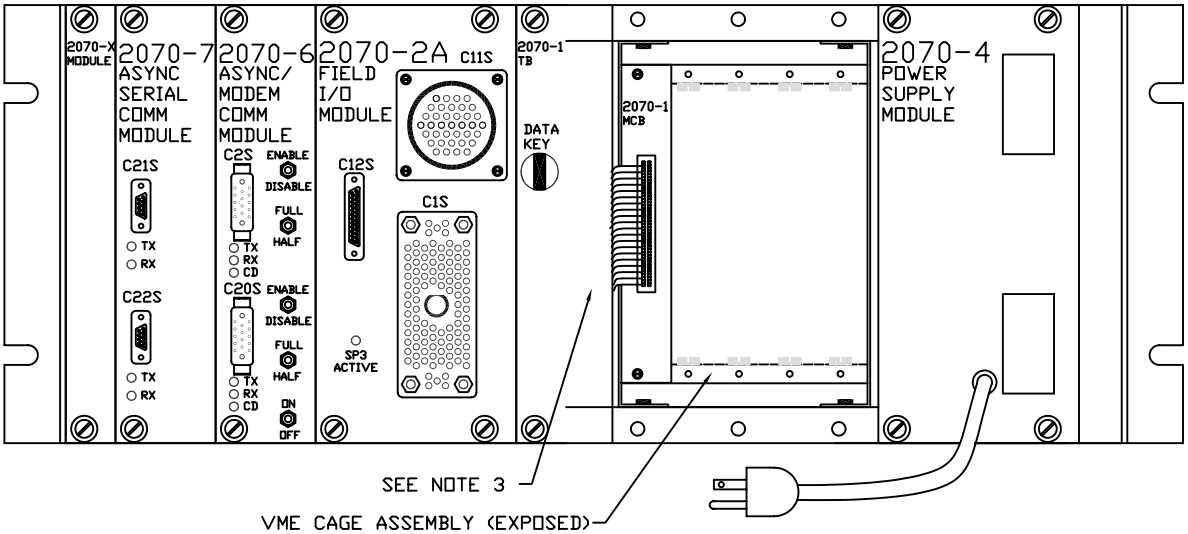
4. The length of the Front Panel Harness shall be no less than 125 mm.

5. A LED indicator for each DC voltage shall be provided.

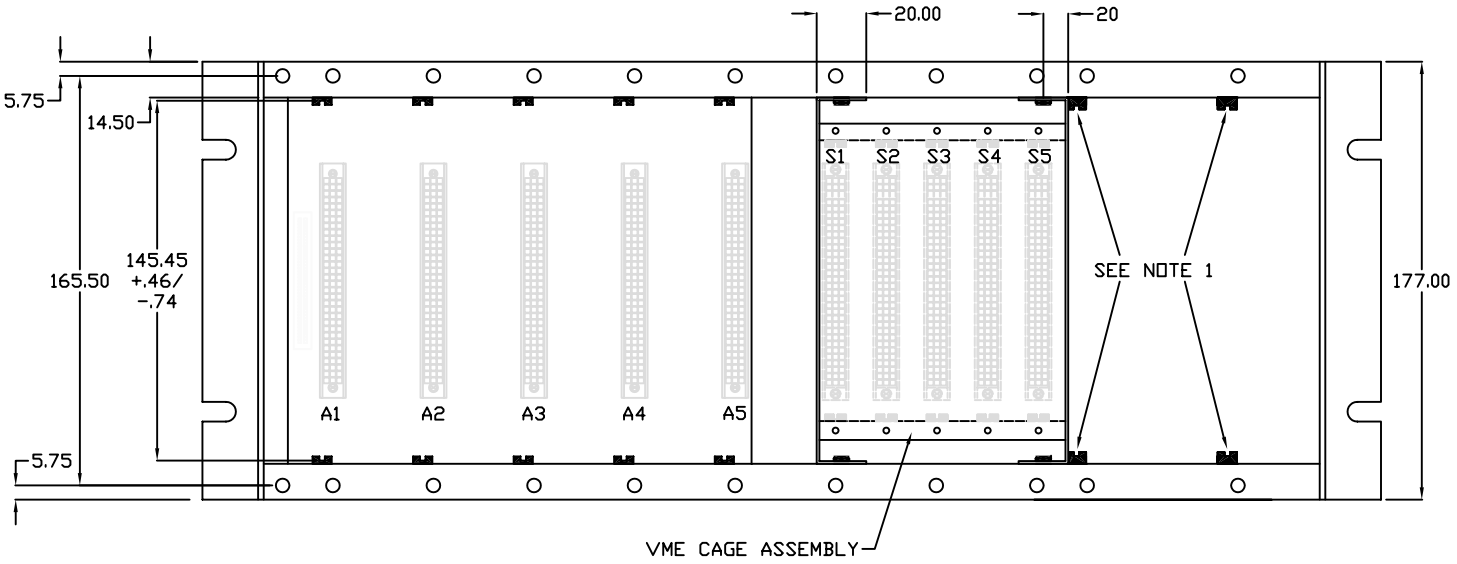
6. With the hinge installed, the distance between the TSD hole center & the CHASSIS Right Side (inside plane) shall be 14.00 mm

TITLE:
MODEL 2070 CHASSIS
FRONT VIEW

NO SCALE
JUNE 8, 2004
9-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

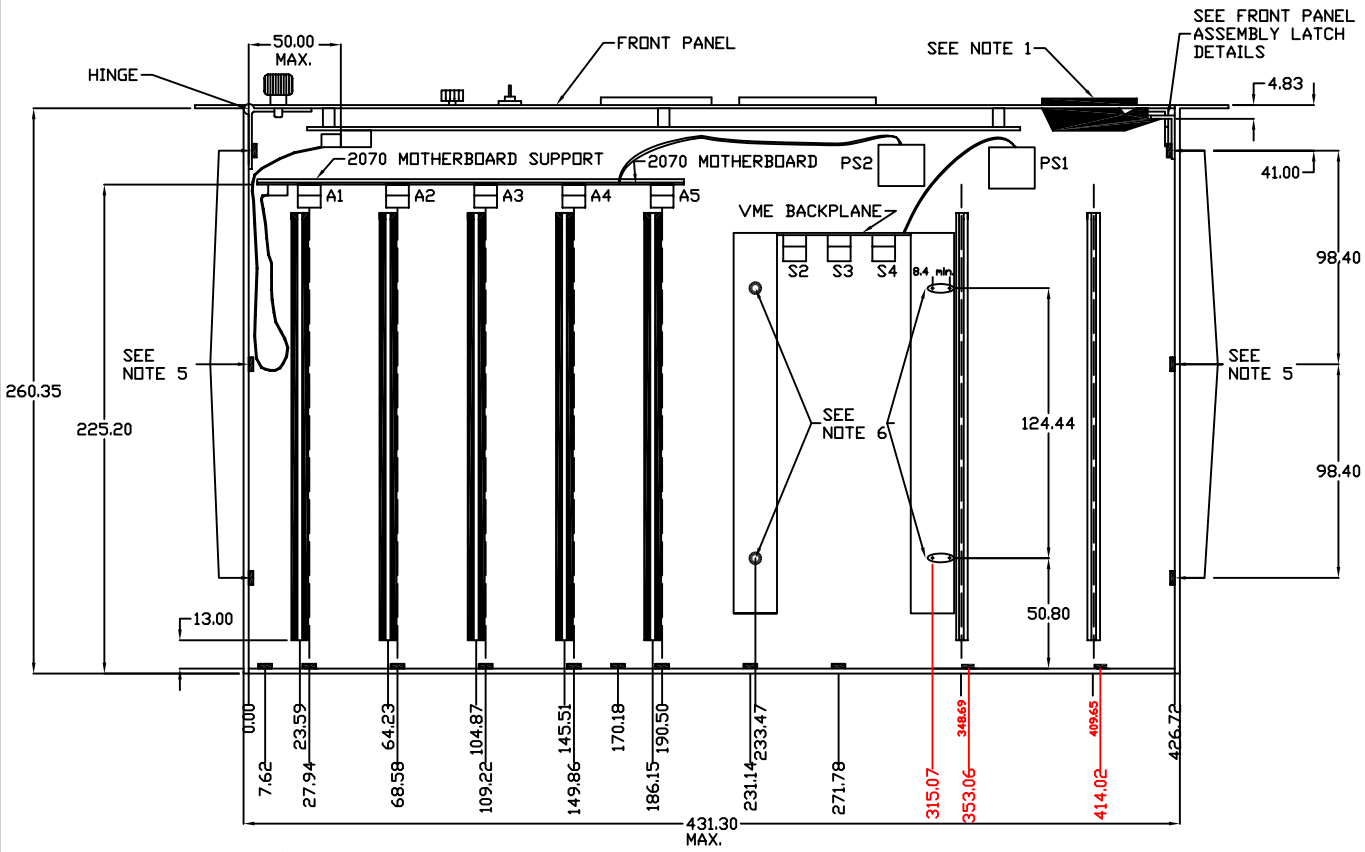
2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

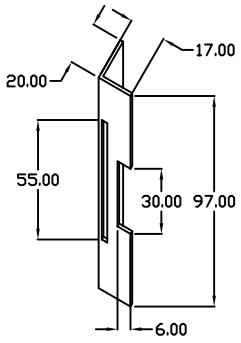
3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

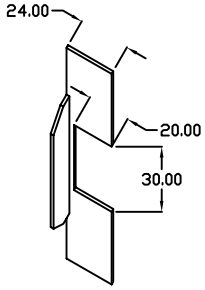
5. Power Supply will be marked with 2070-4A or 2070-4B

TITLE: MODEL 2070 CHASSIS REAR VIEW	
NO SCALE	
JUNE 8, 2004	9-7-2

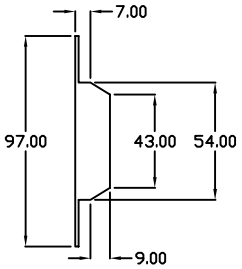




CHASSIS BRACKET



FRONT PANEL BRACKET



SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

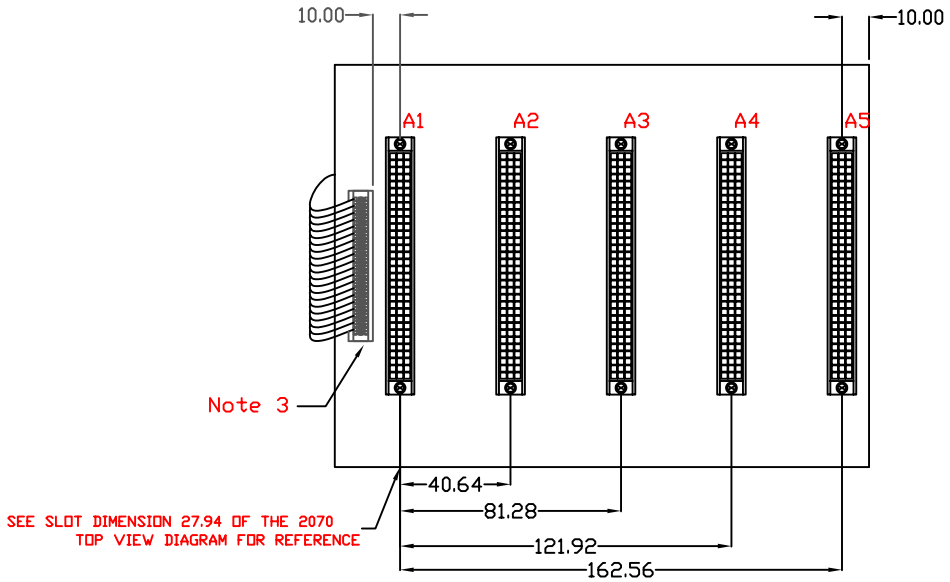
NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 25 mm when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 6.35 mm above unit baseline.
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

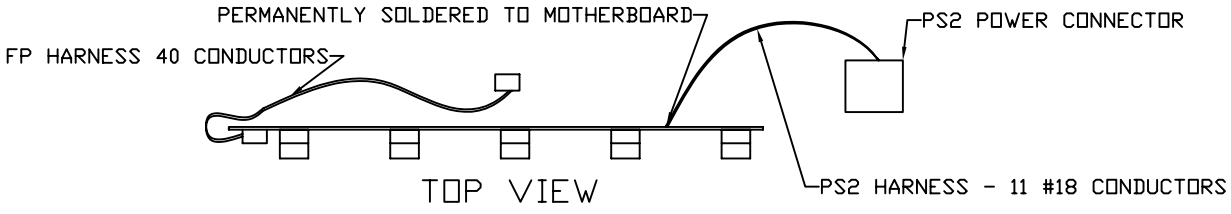
TITLE:

MODEL 2070 CHASSIS TOP VIEW

NO SCALE	
JUNE 8, 2004	9-7-3



CONNECTOR VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The FP Harness shall be connected to the motherboard via a header connector. Pin 1 shall be in the lower right hand corner.

TITLE:

MODEL 2070 CHASSIS MOTHERBOARD

NO SCALE

JUNE 8, 2004

9-7-4

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXC0+	SP5RXD+
6	SP3RTS-	SP3TXC0-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXC0+
20	NA	NA	SP3TXC0-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXC0+	SP3CTS+
16	SP2RTS-	SP2TXC0-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXC0+
20	SP2DCD-	SP2RXC-	SP3TXC0-
21	DCG #1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (NA) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 install, enbales SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

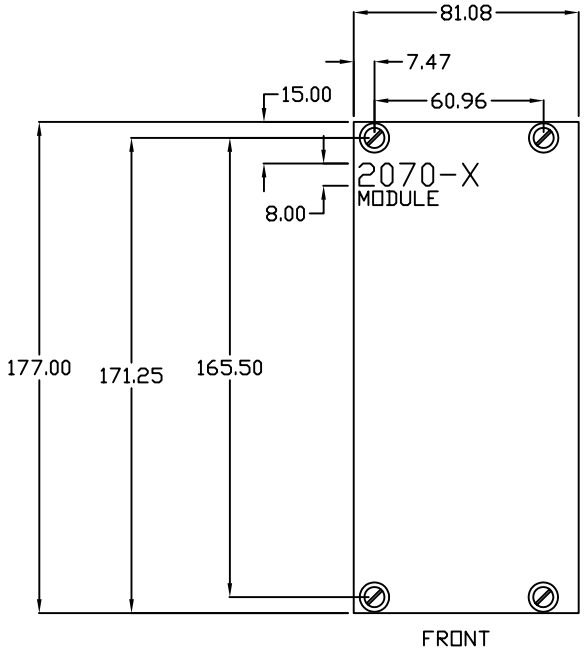
TITLE:

Motherboard A Connector Pin Assignment

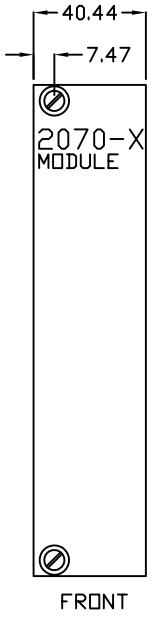
NO SCALE	
JUNE 8, 2004	9-7-5

NOTES (THIS DETAIL)

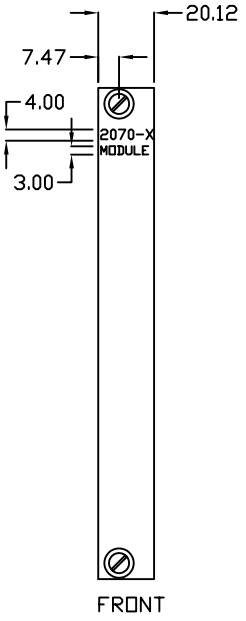
1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL.
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.



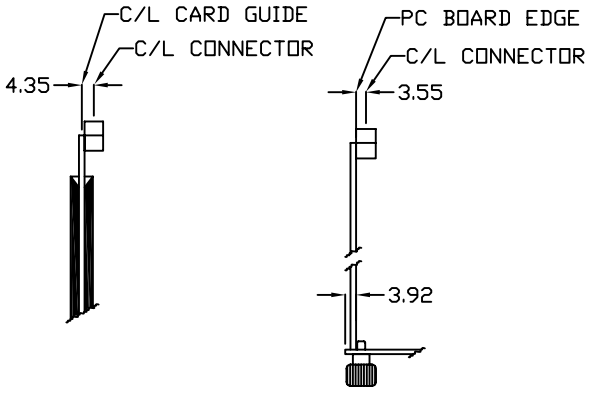
4X WIDE MODULE



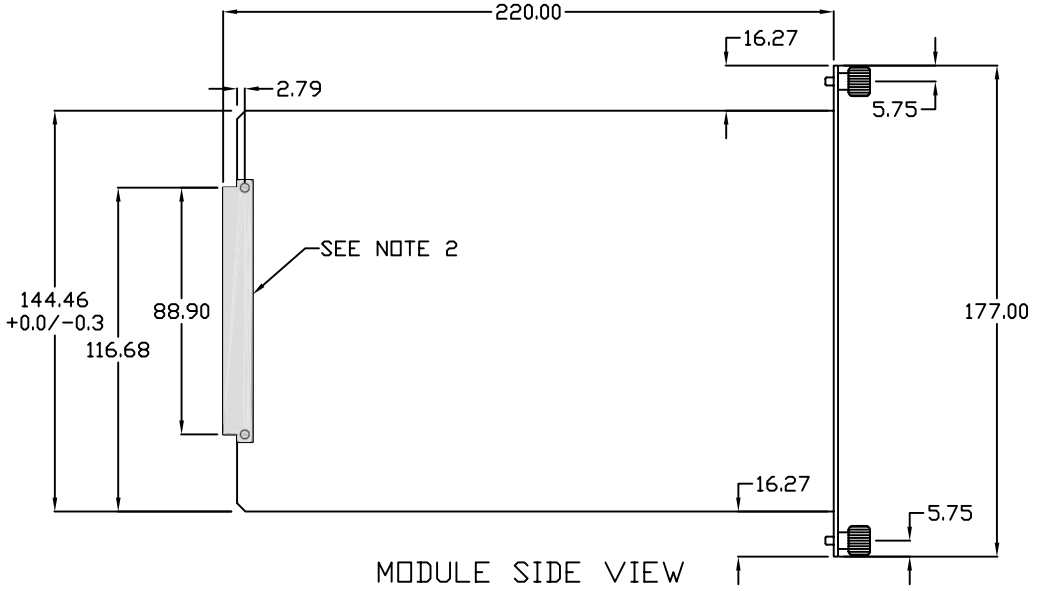
2X WIDE MODULE



1X WIDE MODULE



TOP VIEW DETAILS



MODULE SIDE VIEW

TITLE: MODEL 2070 SYSTEM PCB MODULES, GENERAL

NO SCALE

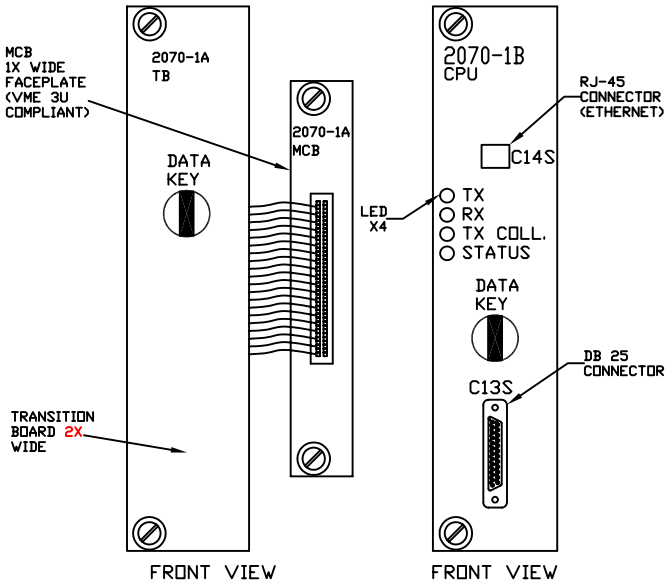
JUNE 8, 2004

9-7-6

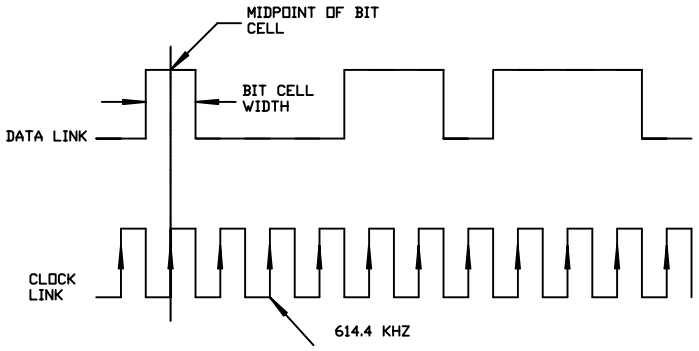
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	NOTE 4	1.2, NOTE 1	ASYNC
SP1S	NOTE 4	19.2, NOTE 2	SYNC, HDLC, SDLC
SP2	SCC2	1.2, NOTE 1	ASYNC
SP2S	SCC2	19.2, NOTE 2	SYNC, HDLC, SDLC
SP3	SCC4	1.2, NOTE 1	ASYNC
SP3S	SCC4	614.4, NOTE 3	SYNC, HDLC, SDLC
SP4	SMC2	9.6, NOTE 1	ASYNC
SP5	SCC3	1.2, NOTE 1	ASYNC
SP5S	SCC3	614.4	SYNC, HDLC, SDLC
SP6	SMC1	38.4, NOTE 1	ASYNC
SP8**	NOTE 4	9.6, NOTE 1	ASYNC
SP8S**	NOTE 4	153.6	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. Additional rates 1.2, 2.4, 4.8, 9.6, 19.2, 38.4.

2. Additional descriptors for other rates:
   SPxSa = 19.2, SPxSb = 38.4, SPxSc = 57.6
   SPxSd = 76.8, SPxSg = 64.0, SPxSe = 153.6.

3. Additional descriptors for other rates:
   SPxSe = 153.6, SPxSf = 614.4.

4. On 2070-1A, SP1 is assigned to 68360 SCC1.
   On 2070-1B, SP1 and SP8 are assigned to the dual SCC, and ETHERNET is assigned to 68EN360 SCC1.

5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

6. ** 2070-1B only.

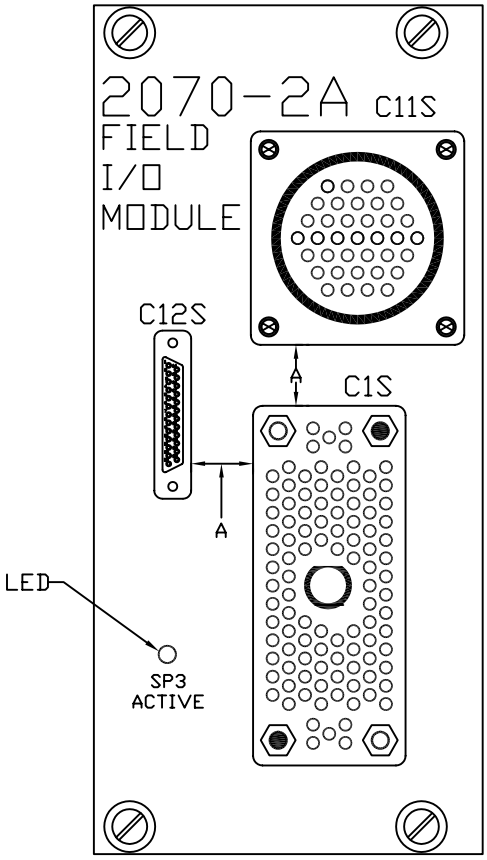
7. BIAS +5VDC refers to voltage required for a Line Terminator device.

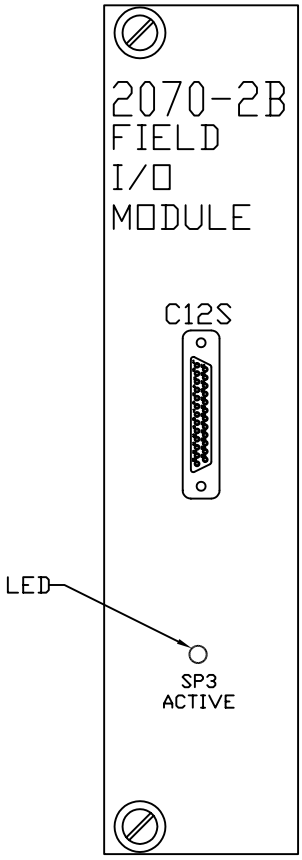
TITLE: MODEL 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL

NO SCALE

JUNE 8, 2004

9-7-7





FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide.
   2070-2B Faceplate shall be 2X wide.
   (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S PIN 12 (+5VDC) IS DERIVED from the Isolated +12 VDC Power Supply.
   BIAS +5VDC refers to voltage required for a LineTerminator device.

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

MODEL 2070-2
FIELD I/O MODULES

NO SCALE

JUNE 8, 2004

9-7-8

C1S PIN ASSIGNMENT

PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	DC GROUND		27	O24	O4-1	53	I14	I2-7	79	I44	I6-5
2	O0	O1-1	28	O25	O4-2	54	I15	I2-8	80	I45	I6-6
3	O1	O1-2	29	O26	O4-3	55	I16	I3-1	81	I46	I6-7
4	O2	O1-3	30	O27	O4-4	56	I17	I3-2	82	I47	I6-8
5	O3	O1-4	31	O28	O4-5	57	I18	I3-3	83	O40	O6-1
6	O4	O1-5	32	O29	O4-6	58	I19	I3-4	84	O41	O6-2
7	O5	O1-6	33	O30	O4-7	59	I20	I3-5	85	O42	O6-3
8	O6	O1-7	34	O31	O4-8	60	I21	I3-6	86	O43	O6-4
9	O7	O1-8	35	O32	O5-1	61	I22	I3-7	87	O44	O6-5
10	O8	O2-1	36	O33	O5-2	62	I23	I3-8	88	O45	O6-6
11	O9	O2-2	37	O34	O5-3	63	I28	I4-5	89	O46	O6-7
12	O10	O2-3	38	O35	O5-4	64	I29	I4-6	90	O47	O6-8
13	O11	O2-4	39	I0	I1-1	65	I30	I4-7	91	O48	O7-1
14	DC GROUND		40	I1	I1-2	66	I31	I4-8	92	DC GROUND	
15	O12	O2-5	41	I2	I1-3	67	I32	I5-1	93	O49	O7-2
16	O13	O2-6	42	I3	I1-4	68	I33	I5-2	94	O50	O7-3
17	O14	O2-7	43	I4	I1-5	69	I34	I5-3	95	O51	O7-4
18	O15	O2-8	44	I5	I1-6	70	I35	I5-4	96	O52	O7-5
19	O16	O3-1	45	I6	I1-7	71	I36	I5-5	97	O53	O7-6
20	O17	O3-2	46	I7	I1-8	72	I37	I5-6	98	O54	O7-7
21	O18	O3-3	47	I8	I2-1	73	I38	I5-7	99	O55	O7-8
22	O19	O3-4	48	I9	I2-2	74	I39	I5-8	100	O36	O5-5
23	O20	O3-5	49	I10	I2-3	75	I40	I6-1	101	O37	O5-6
24	O21	O3-6	50	I11	I2-4	76	I41	I6-2	102	O38 DET RES	O5-7
25	O22	O3-7	51	I12	I2-5	77	I42	I6-3	103	O39 WDT	O5-8
26	O23	O3-8	52	I13	I2-6	78	I43	I6-4	104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION		PIN	FUNCTION	
	NAME	PORT		NAME	PORT		NAME	PORT		NAME	PORT
1	O56	O8-1	11	I25	I4-2	21	I54	I7-7	31	DC GROUND	
2	O57	O8-2	12	I26	I4-3	22	I55	I7-8	32	NA	- - -
3	O58	O8-3	13	I27	I4-4	23	I56	I8-1	33	NA	- - -
4	O59	O8-4	14	DC GROUND		24	I57	I8-2	34	NA	- - -
5	O60	O8-5	15	I48	I7-1	25	I58	I8-3	35	NA	- - -
6	O61	O8-6	16	I49	I7-2	26	I59	I8-4	36	NA	- - -
7	O62	O8-7	17	I50	I7-3	27	I60	I8-5	37	DC GROUND	
8	O63	O8-8	18	I51	I7-4	28	I61	I8-6			
9	DC GROUND		19	I52	I7-5	29	I62	I8-7			
10	I24	I4-1	20	I53	I7-6	30	I63	I8-8			

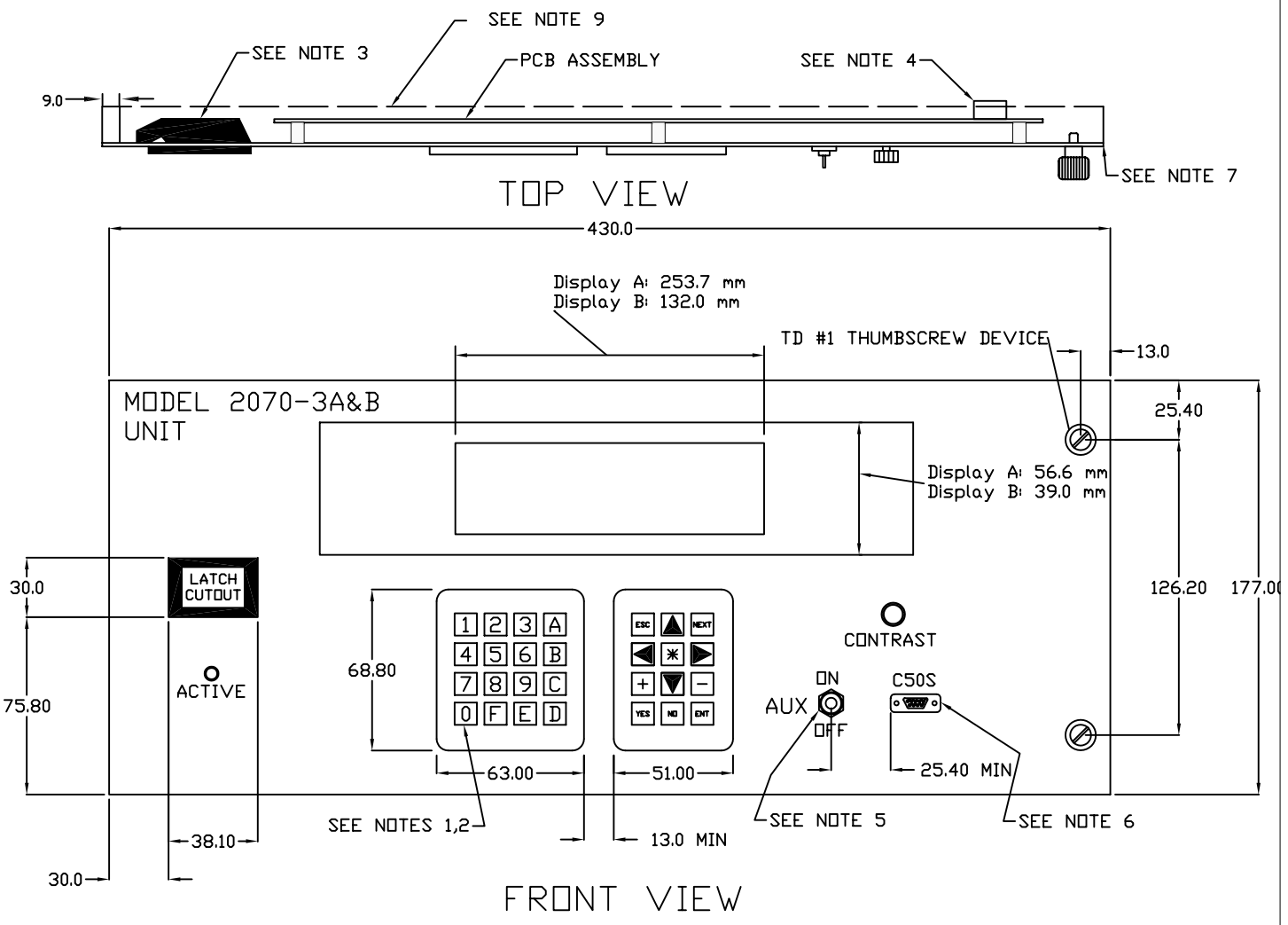
TITLE:

MODEL 2070-2A
FIELD I/O MODULE
C1 & C11 CONNECTORS

NO SCALE

JUNE 8, 2004

9-7-9



NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. The 40 contact connector shall be compatible to the FP harness in type & pin assignments. Center of the FP harness connector shall be vertically positioned 90 +/- 5 mm as measured from the top of the FPA. The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Front panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
10. C60P B Box Power +5VDC, 350mA max. with an isolated Interface Ground #3

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	B Box Power, Note 10
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #3
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:

MODEL 2070-3A&B FRONT PANEL ASSEMBLY

NO SCALE	9-7-10
JUNE 8, 2004	

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	0D

TITLE:

MODEL 2070-3
FRONT PANEL ASSEMBLY
KEY CODES

NO SCALE

JUNE 8, 2004

9-7-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Pn = 0 : Clear Tab at Currrent Position, Pn = 3 : Clear All Tabs
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B.
Commands code shall be available for option 3C (C60P).

INQUIRY COMMAND-RESPONSE CODES

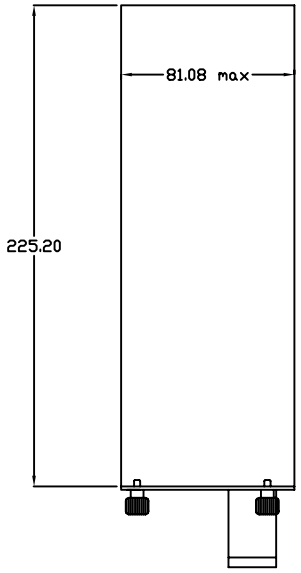
COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

MODEL 2070-2
FIELD I/O MODULES

NO SCALE

JUNE 8, 2004

9-7-12



TOP VIEW

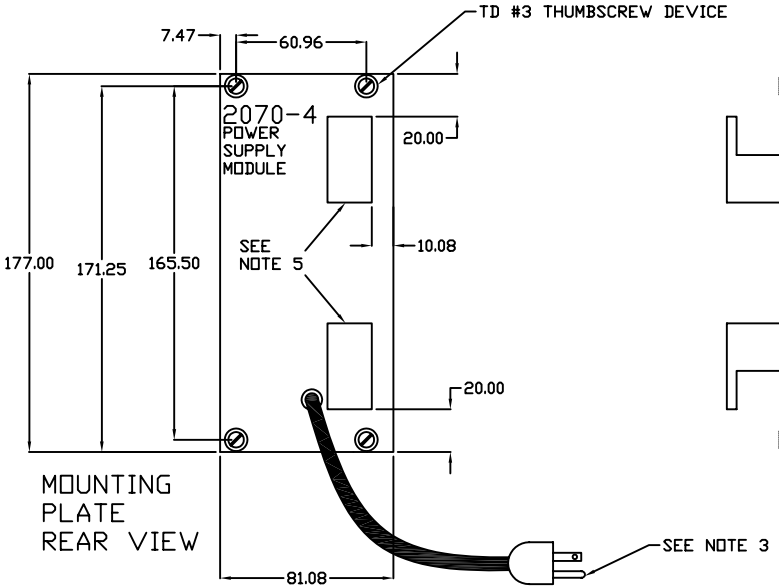
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC
7	DC GROUND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

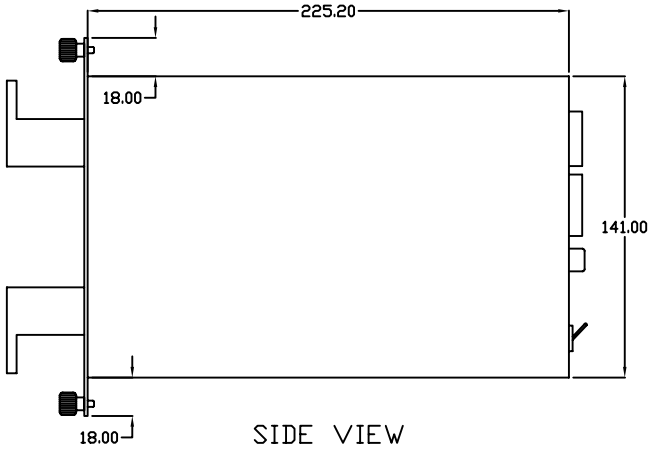
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

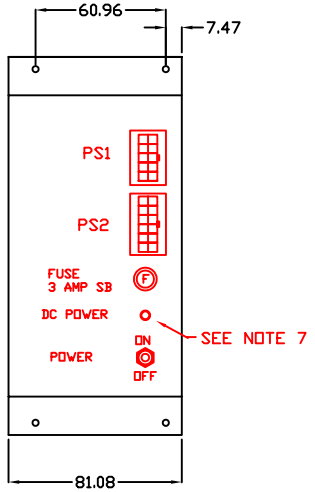
   PS1 connector shall be a 10 position PLUG connector.
   PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, +12 ISO, +12 SERIAL, -12 SERIAL).
8. Power Supply will be marked with 2070-4A or 2070-4B



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



FRONT VIEW

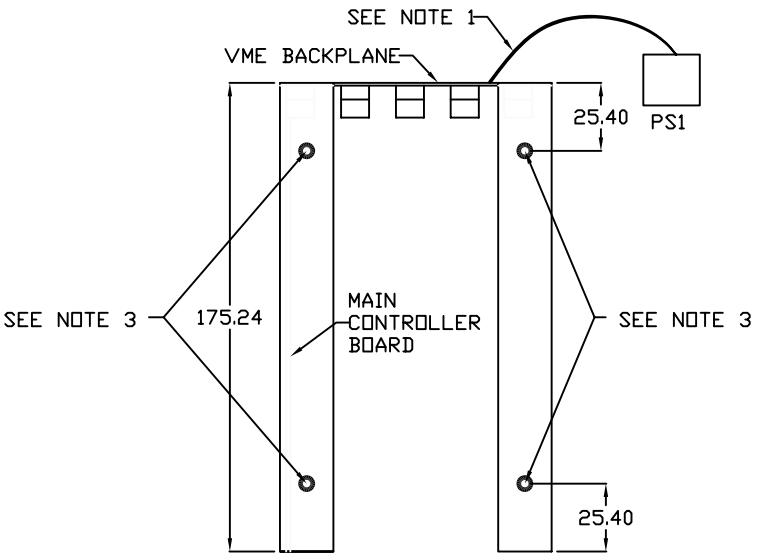
TITLE:

MODEL 2070-4
POWER SUPPLY MODULE

NO SCALE

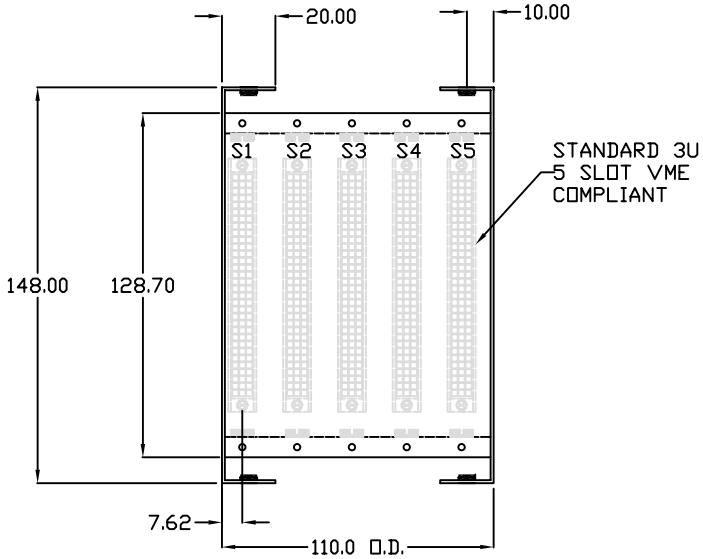
JUNE 8, 2004

9-7-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. G-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

TITLE:

MODEL 2070-5
VME CAGE ASSEMBLY

NO SCALE	
JUNE 8, 2004	9-7-14